



正基科技股份有限公司


SPECIFICATION

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PRODUCT NAME : AP6234

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW		APPROVED	DCC ISSUE
	PM	QA		
Beth	Mandy	Carol	Richard	

AMPAK

AP6234

WiFi 11a/b/g/n +Bluetooth 4.0
SIP Module Spec Sheet

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Revision History

Date	Revision Content	Revised By	Version
2012/10/18	- Initial released	Brian	1.0
2012/12/18	- Pin definition modify	Joe	1.1
2013/01/23	- Pin definition modify	Joe	1.2
2013/04/26	- Specification modify	Joe	1.3
2013/10/12	- Block Diagram modify	Brian	1.4
2014/09/16	- Pin definition modify	Brian	1.5
2014/12/16	- Pin definition modify for LTE Coex	Brian	1.6
2016/03/29	- Specification modify - Add Reflow Suggestion and MLS	Richard	1.7
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1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module, with integrated dual band (2.4GHz/5GHz) IEEE 802.11 a/b/g and single-stream IEEE 802.11n MAC/baseband/radio and Bluetooth 4.0.

The integrated module provides SDIO V2.0 Host interface for Wi-Fi, high-speed UART is provided for the Bluetooth Host interface.

This compact module is a total solution for a combination of Wi-Fi dual mode + BT4.0 technologies. The module is specifically developed for mobiles, tablets or handheld wireless system devices.

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2. Features

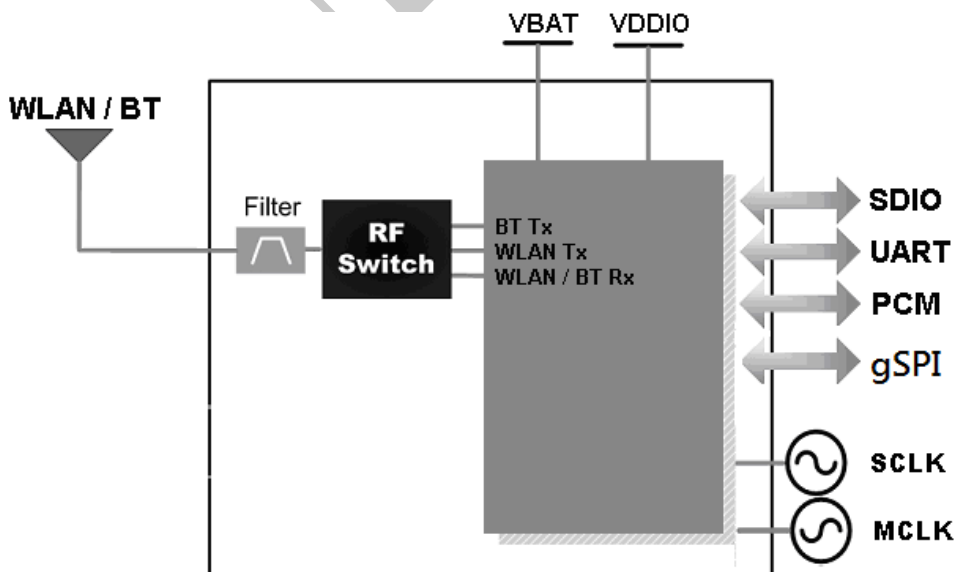
IEEE 802.11x Key Features

- Dual-band 2.4GHz/5GHz 802.11a/b/g/n.
- Single-stream IEEE 802.11n support for 20MHz and 40MHz channels provides PHY layer rates up to 150Mbps.
- WLAN host interface options: SDIO v2.0 — up to 50 MHz clock rate
- Support a single antenna shared between WLAN and Bluetooth.
- Security: WEP, WPS, WPA, WPA2, WMM, WAPI, AES,...

Bluetooth Features

- Bluetooth V4.0(BLE) Low Energy with provisions for supporting future specifications.
- Bluetooth Class1 or Class2 transmitter operation.
- BT host digital interface UART(up to 4 Mbps) with support all Bluetooth4.0 package types
- Multipoint operation with up to seven active ACL links, three active SCO and eSCO connections.
- Full support for power savings modes (standard sniff, deep sleep modes)
- ECI - enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

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4. General Specification

4.1 General Specification

Model Name	AP6234
Product Description	Supports Wi-Fi dual mode /Bluetooth functionalities
Dimension	L x W x H: 12.0 x 12.0 x 1.5 (typical) mm
WiFi Interface	SDIOV2.0 / gSPI
BT Interface	UART/ PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.6	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.6	4.8	V
VDDIO	1.6	3.3	3.4	V

5. WiFi RF Specification

5.1 2.4GHz & 5GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11a/b/g/n, WiFi compliant
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band) 4.900 GHz ~ 5.845 GHz (5.0 GHz ISM Band)
Number of Channels	2.4GHz : Ch1 ~ Ch14 5.0GHz : Please see the table ¹
Modulation	802.11a : OFDM /64-QAM, 16-QAM, QPSK, BPSK 802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM, 16-QAM, QPSK, BPSK
Output Power	802.11a /54Mbps : 13 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11an /MCS7@20MHz : 12 dBm ± 1.5 dB @ EVM ≤ -27dB
	802.11an /MCS7@40MHz : 11 dBm ± 1.5 dB @ EVM ≤ -27dB
	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11gn /MCS7@20MHz : 14 dBm ± 1.5 dB @ EVM ≤ -27dB
Receive Sensitivity (11GN) @20MHz @10% PER	- MCS=0 PER @ -88 dBm, typical
	- MCS=1 PER @ -84 dBm, typical
	- MCS=2 PER @ -82 dBm, typical
	- MCS=3 PER @ -80 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -74dBm, typical
	- MCS=6 PER @ -72 dBm, typical
	- MCS=7 PER @ -70 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -88 dBm, typical
	- 9Mbps PER @ -87 dBm, typical
	- 12Mbps PER @ -85 dBm, typical
	- 18Mbps PER @ -83 dBm, typical
	- 24Mbps PER @ -81 dBm, typical
	- 36Mbps PER @ -77 dBm, typical
	- 48Mbps PER @ -74 dBm, typical
	- 54Mbps PER @ -72 dBm, typical
Receive Sensitivity	- 1Mbps PER @ -95 dBm, typical

(11b) @8% PER	- 2Mbps PER @ -94 dBm, typical
	- 5.5Mbps PER @ -90 dBm, typical
	- 11Mbps PER @ -87 dBm, typical
Receive Sensitivity (11a) @10% PER	- 6Mbps PER @ -86 dBm, typical
	- 9Mbps PER @ -84 dBm, typical
	- 12Mbps PER @ -82 dBm, typical
	- 18Mbps PER @ -80 dBm, typical
	- 24Mbps PER @ -78 dBm, typical
	- 36Mbps PER @ -76 dBm, typical
	- 48Mbps PER @ -73 dBm, typical
Receive Sensitivity (11AN)@20MHz @10% PER	- MCS=0 PER @ -85 dBm, typical
	- MCS=1 PER @ -82 dBm, typical
	- MCS=2 PER @ -80 dBm, typical
	- MCS=3 PER @ -78 dBm, typical
	- MCS=4 PER @ -75 dBm, typical
	- MCS=5 PER @ -70 dBm, typical
	- MCS=6 PER @ -69 dBm, typical
	- MCS=7 PER @ -67 dBm, typical
Receive Sensitivity (11AN)@40MHz @10% PER	- MCS=0 PER @ -83 dBm, typical
	- MCS=1 PER @ -80 dBm, typical
	- MCS=2 PER @ -78 dBm, typical
	- MCS=3 PER @ -76 dBm, typical
	- MCS=4 PER @ -73 dBm, typical
	- MCS=5 PER @ -68 dBm, typical
	- MCS=6 PER @ -66 dBm, typical
	- MCS=7 PER @ -65 dBm, typical

5GHz Channel table

Band (GHz)	Operating Channel Numbers	Channel center frequencies(MHz)
5.15GHz~5.25GHz	36	5180
	40	5200
	44	5220
	48	5240
5.25GHz~5.35GHz	52	5260
	56	5280
	60	5300
	64	5320
5.5GHz~5.7GHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
5.725GHz~5.825GHz	140	5700
	149	5745
	153	5765
	157	5785
	161	5805

6. Bluetooth Specification

6.1 Bluetooth Specification

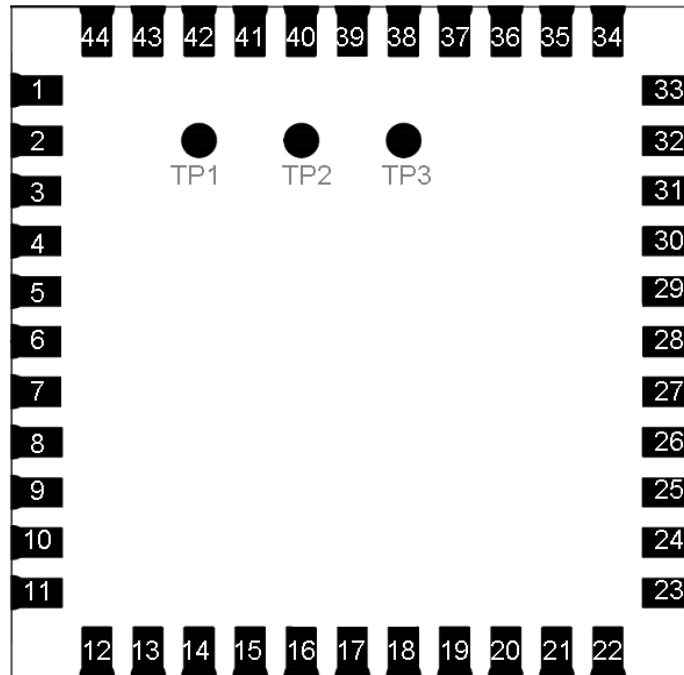
Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V4.0 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2.400 GHz ~ 2483.5 GHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
RF Specification			
	Min.	Typical.	Max.
Output Power (Class 1.5)		8 dBm	
Output Power (Class 2)		2 dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

7. Pin Assignments

7.1 Pin Outline

< TOP VIEW >



7.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	NC	—	Floating (Don't connected to ground)
5	WL_GPIO5	I/O	WLAN Priority GPIO for LTE Coex
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	WL_GPIO3	I/O	WiFi GPIO for LTE TX Coex
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	XTAL oscillator input
11	XTAL_OUT	O	XTAL oscillator output
12	WL_REG_ON	I	Internal regulators power enable/disable
13	WL_HOST_WAKE	O	WLAN to wake-up HOST

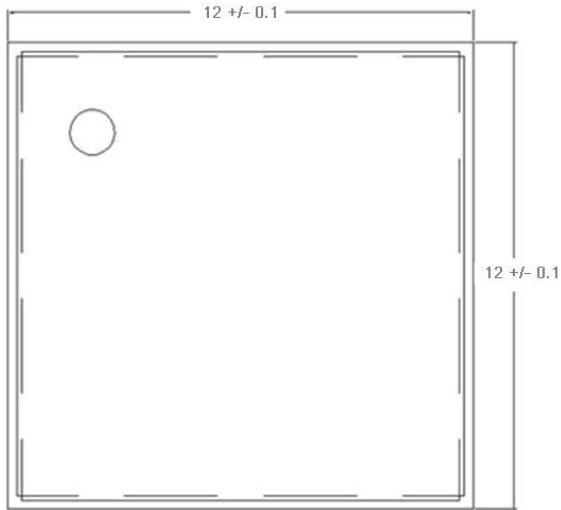
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	Low power oscillator clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	MODE_SELECTION	I/O	Mode selection GPIO: 1. Default pin floating is SDIO mode. 2. Pull high is gSPI mode.
30	NC	—	Floating (Don't connected to ground)
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	BT_RST_N	I	Low asserting reset for Bluetooth core
35	NC	—	Floating (Don't connected to ground)
36	GND	—	Ground connections
37	NC	—	Floating (Don't connected to ground)
38	NC	—	Floating (Don't connected to ground)
39	NC	—	Floating (Don't connected to ground)
40	NC	—	Floating (Don't connected to ground)
41	UART_RTS_N	O	Bluetooth UART interface
42	UART_TXD	O	Bluetooth UART interface
43	UART_RXD	I	Bluetooth UART interface
44	UART_CTS_N	I	Bluetooth UART interface
45	TP1	—	Floating (Don't connected to ground)
46	TP2	—	Floating (Don't connected to ground)
47	TP3	—	Floating (Don't connected to ground)

8. Dimensions

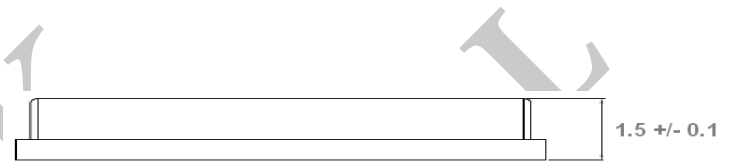
8.1 Physical Dimensions

(Unit: mm)

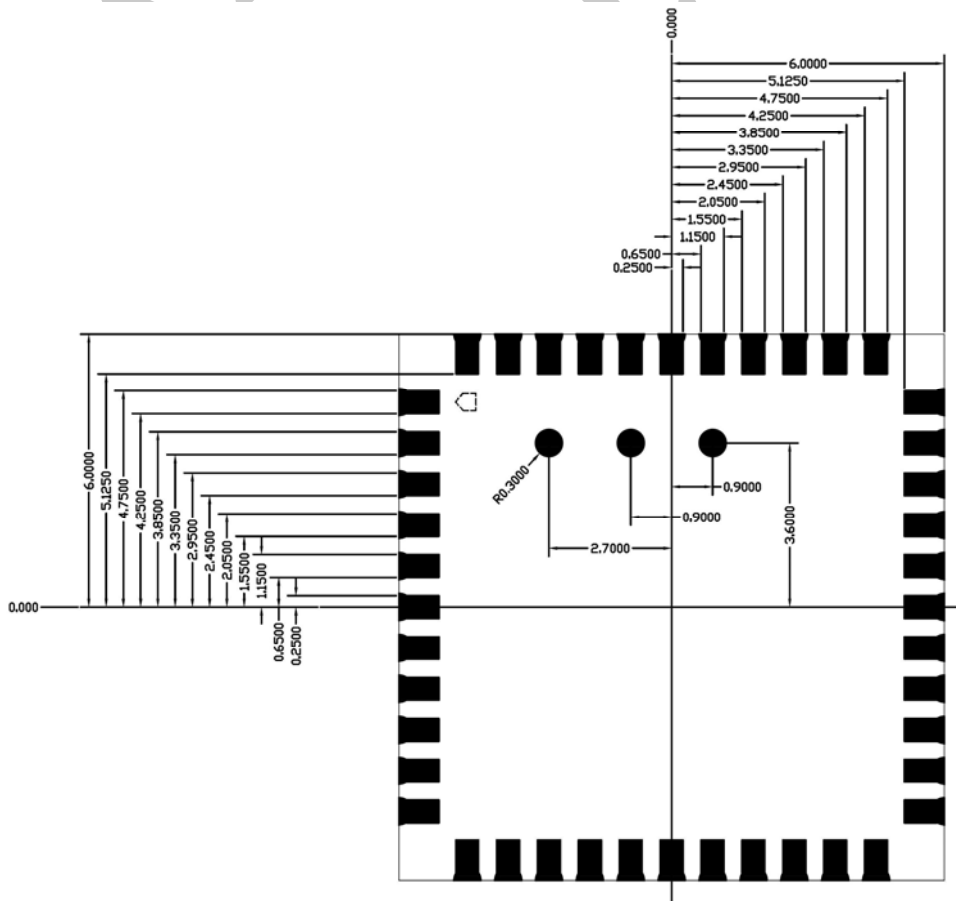
< TOP VIEW >



< Side View >



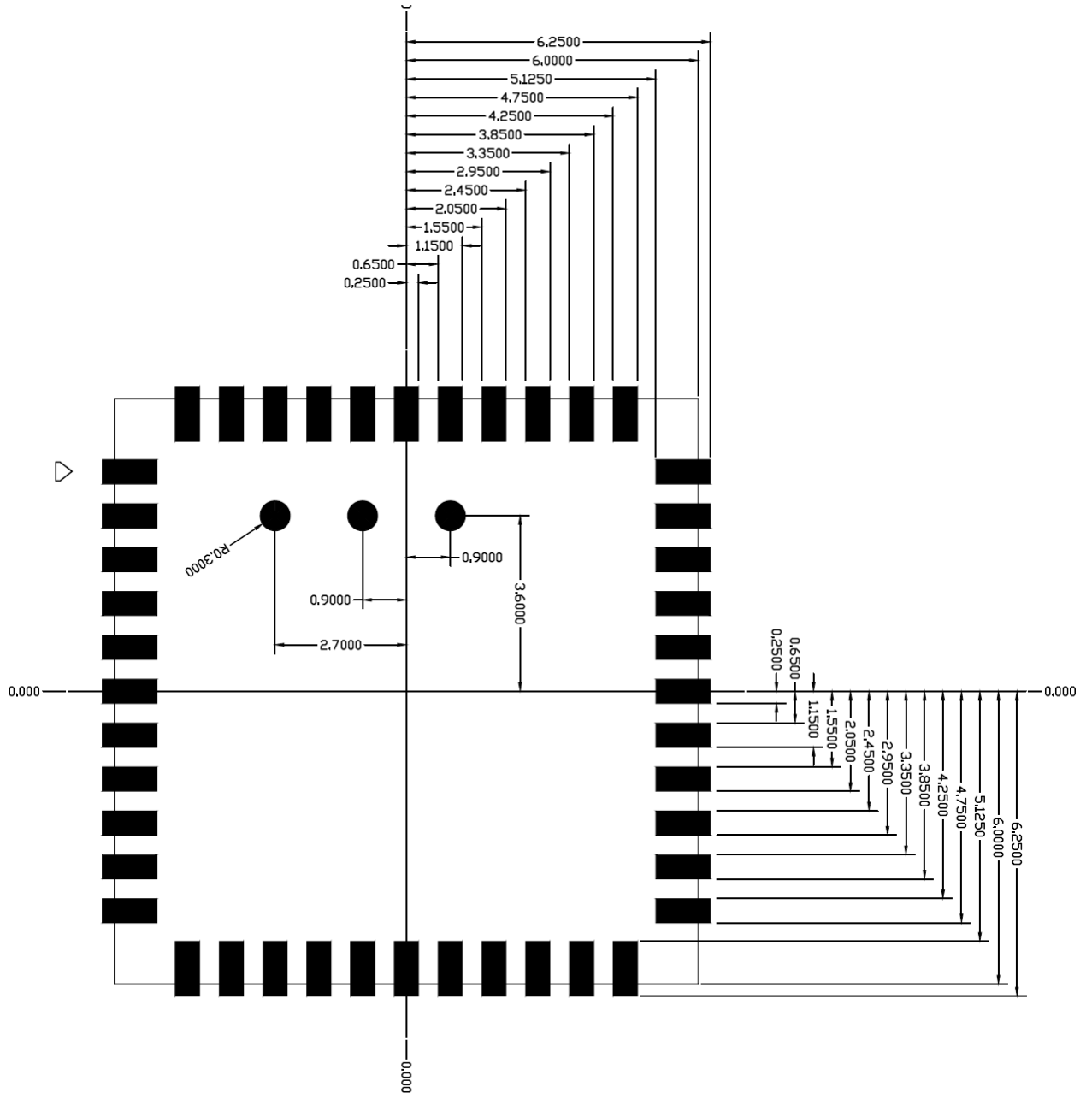
< TOP VIEW >



8.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >



9. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

9.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

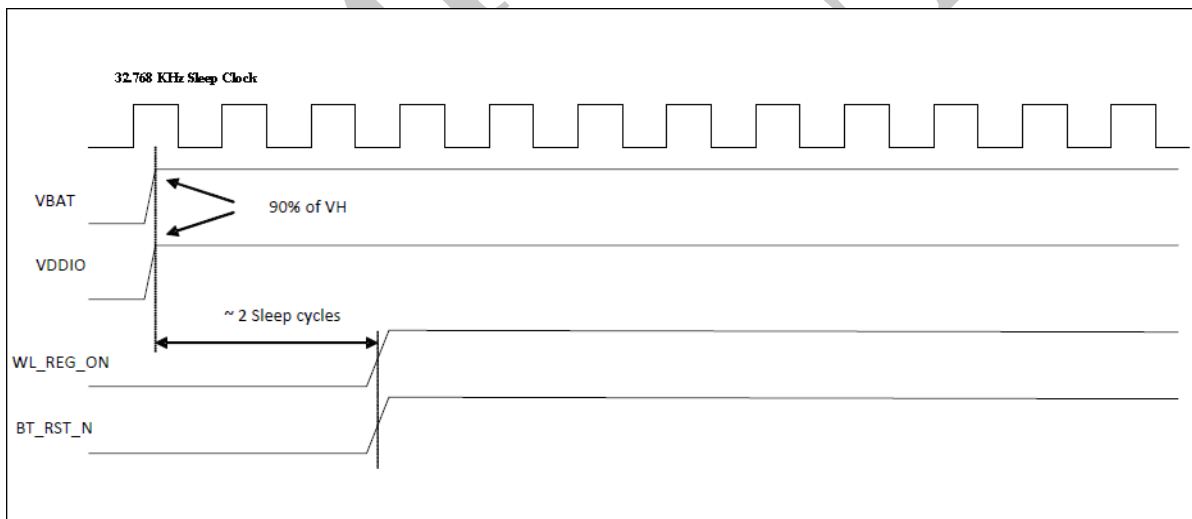
10. Host Interface Timing Diagram

10.1 Power-up Sequence Timing Diagram

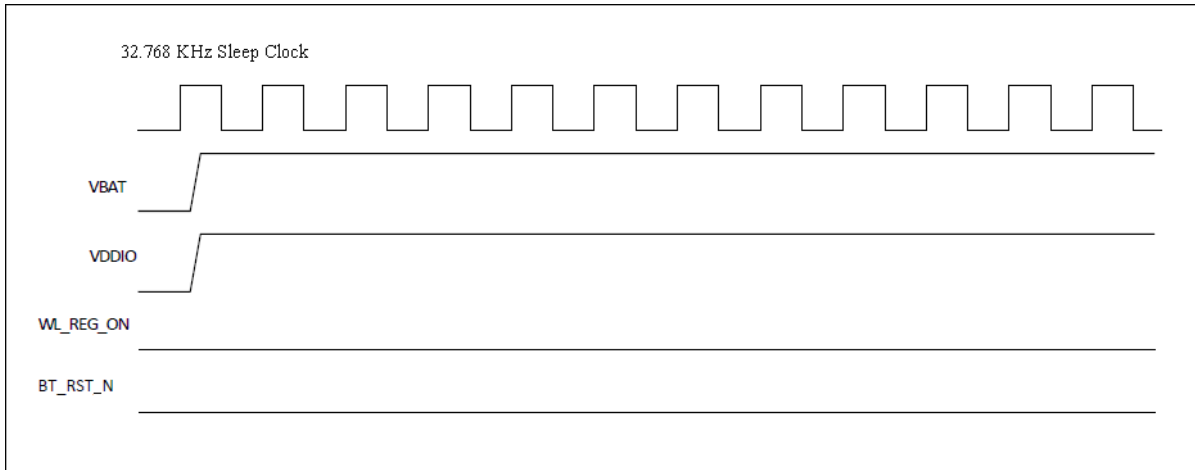
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

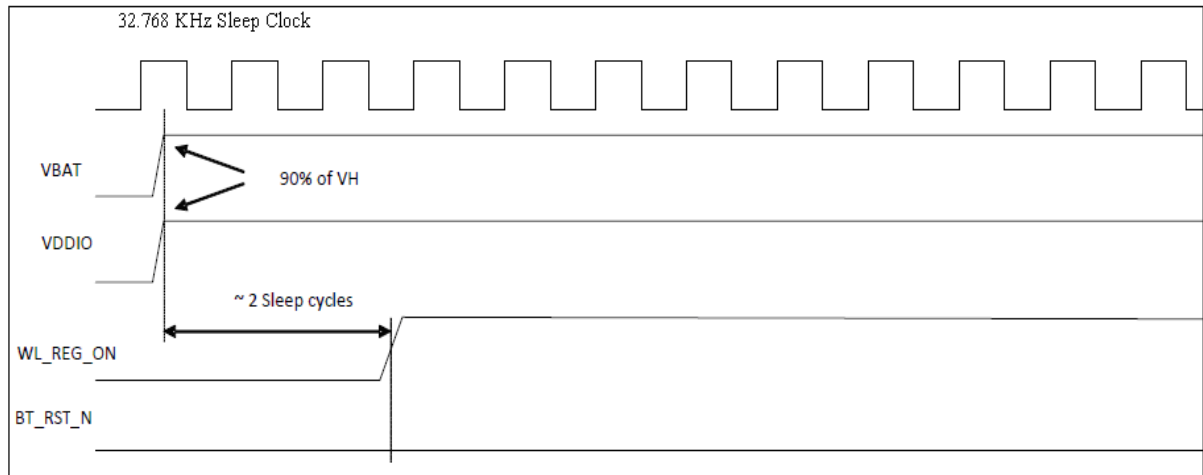
- ※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT_RST_N: Low asserting reset for Bluetooth only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



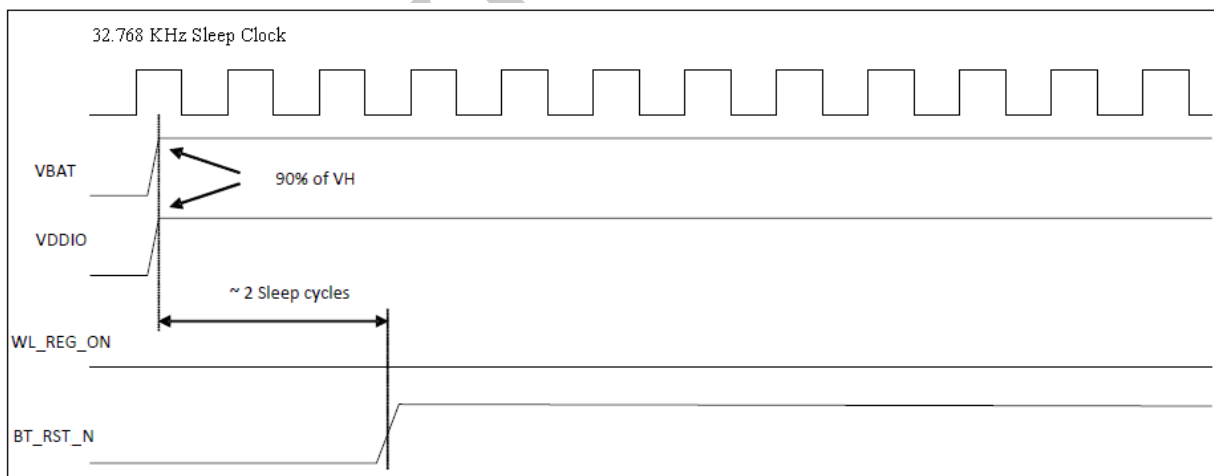
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

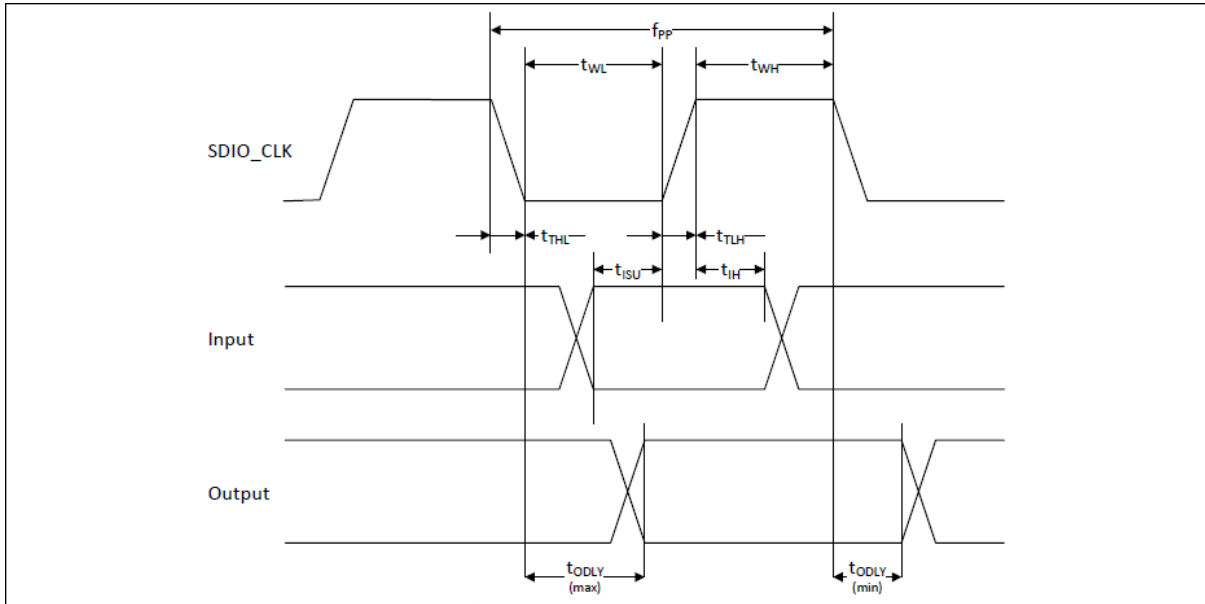


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

10.2 SDIO Default Mode Timing Diagram

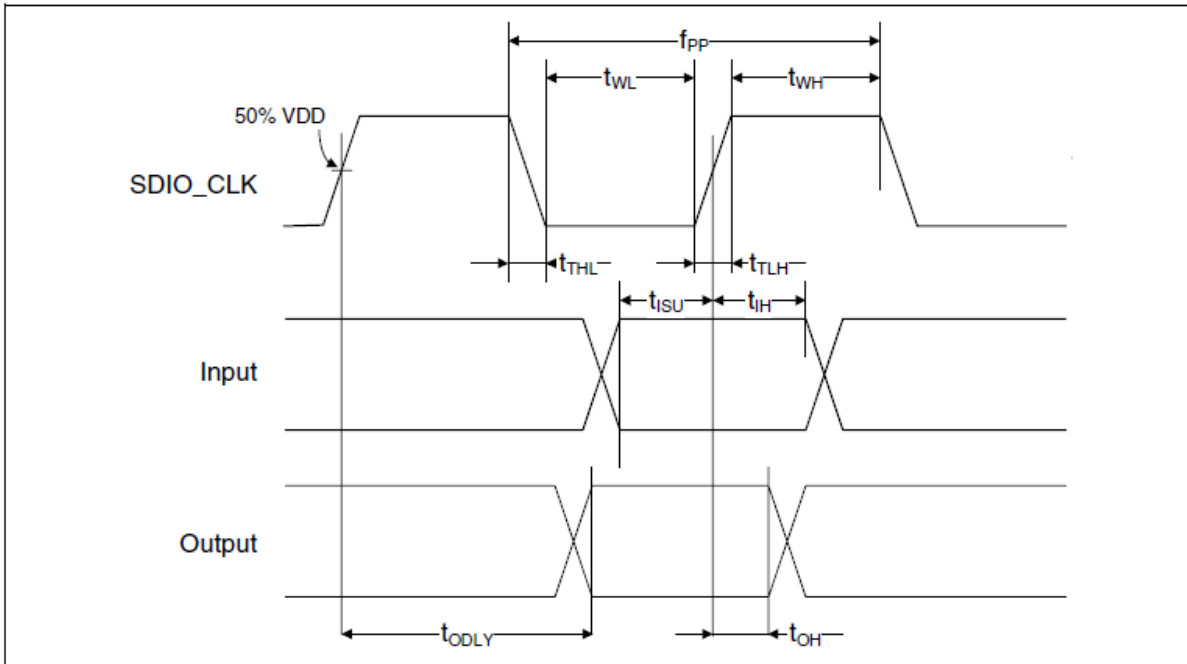


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	0	-	14	ns
Output delay time - Identification mode	tODLY	0	-	50	ns

a. Timing is based on $CL \leq 40pF$ load on CMD and Data.

b. $\min(V_{ih}) = 0.7 \times V_{DDIO}$ and $\max(V_{il}) = 0.2 \times V_{DDIO}$.

10.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency-Data Transfer mode	f_{PP}	0	-	50	MHz
Frequency-Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	7	-	-	ns
Clock high time	t_{WH}	7	-	-	ns
Clock rise time	t_{TLH}	-	-	3	ns
Clock low time	t_{TLH}	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6	-	-	ns
Input hold time	t_{IH}	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	-	-	14	ns
Output hold time	t_{OH}	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on $CL \leq 40pF$ load on CMD and Data.

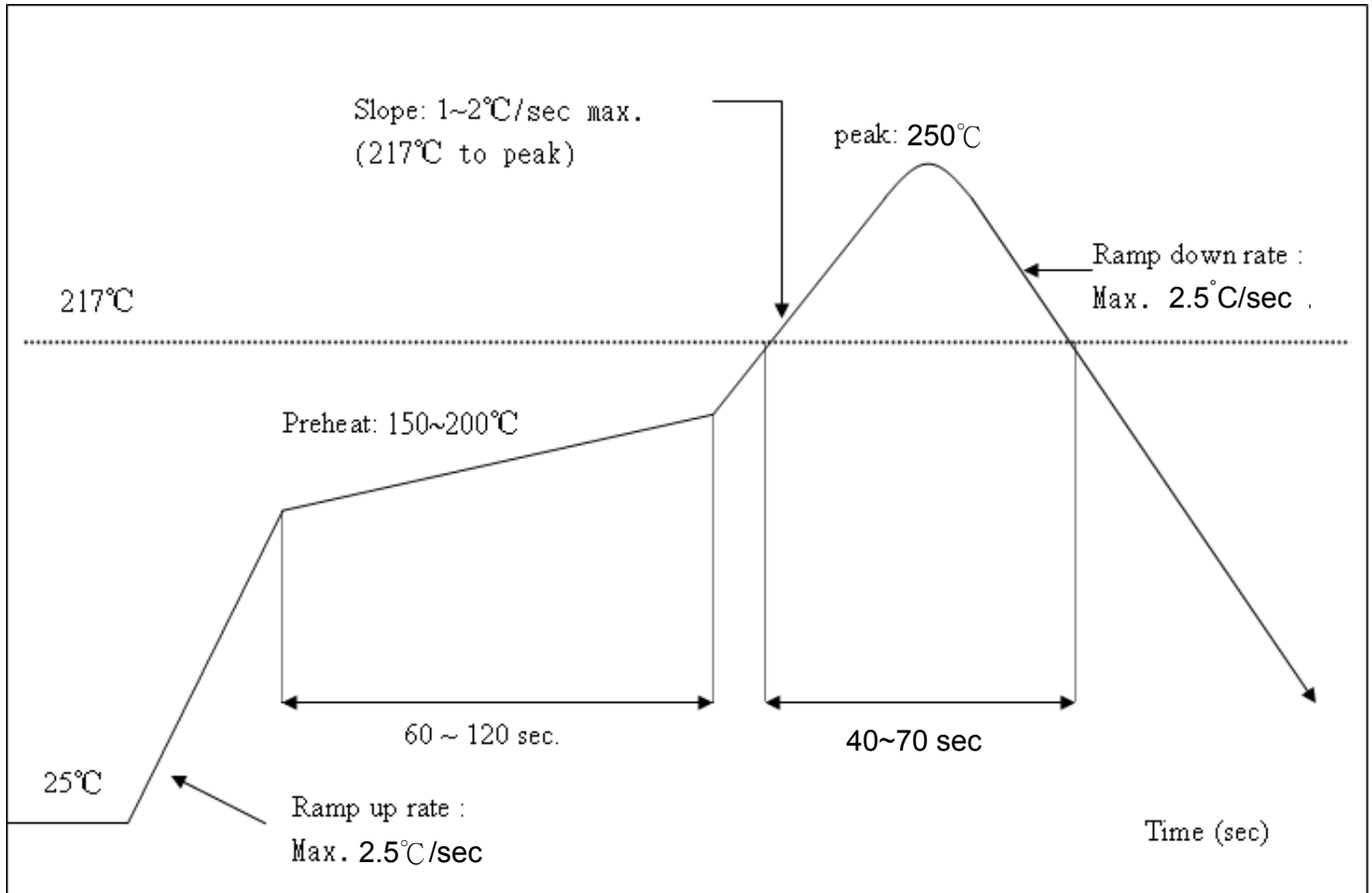
b. $\min(V_{ih}) = 0.7 \times V_{DDIO}$ and $\max(V_{il}) = 0.2 \times V_{DDIO}$.

11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



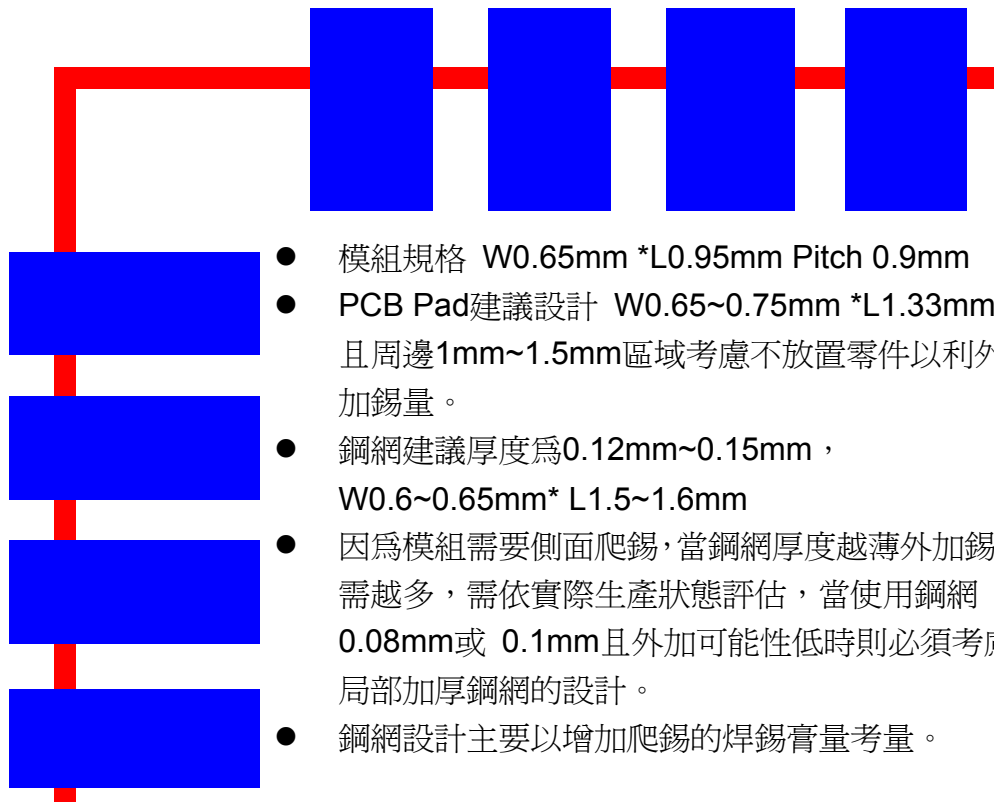
The notification of WiFi module before mounting:

The aperture of stencil should be larger than foot print of module, and the stencil thickness should be not less than 0.12mm.

Reflow 時需使用 N2, 含氧量建議 5000 ppm 以下,

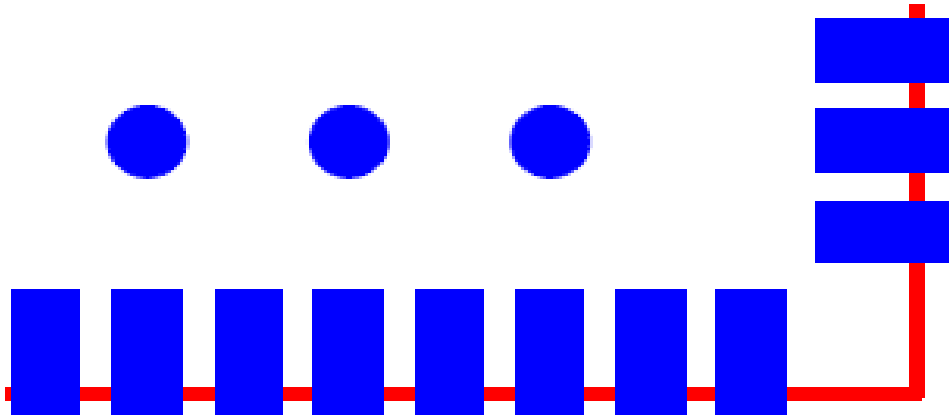
It must use N2 for reflow and suggest the concentration of oxygen less than 5000 ppm .

Solder Paste definition



- 模組規格 W0.65mm *L0.95mm Pitch 0.9mm
- PCB Pad建議設計 W0.65~0.75mm *L1.33mm , 且周邊1mm~1.5mm區域考慮不放置零件以利外加錫量。
- 鋼網建議厚度為0.12mm~0.15mm , W0.6~0.65mm* L1.5~1.6mm
- 因為模組需要側面爬錫，當鋼網厚度越薄外加錫量需越多，需依實際生產狀態評估，當使用鋼網 0.08mm或 0.1mm且外加可能性低時則必須考慮局部加厚鋼網的設計。
- 鋼網設計主要以增加爬錫的焊錫膏量考量。

- Module Specifications : W:0.65mm * L:0.95mm pitch 0.9 mm
- The proposed design W:0.65~0.75 mm * L:1.33mm. Consider not place other parts in the peripheral area of 1 mm ~ 1.5 mm to facilitate additional amount of solder for PCB pad.
- We Suggest the thickness of Stencil between 0.12 mm ~0.15mm, the W between 0.6~0.65mm and the L between L1.5~1.6mm.
- If the thickness of the stencil is thinner, we suggest to adding more solder, to increase the wetting ability. Depends on different production situation, if the stencil thickness is 0.08~0.1mm, and the module nearby area is no more space for expending soldering area, we will suggest to increase the stencil thickness to increase the wetting ability.
- The major consideration parts of stencil design is to increase the solder paste wetting ability.



模組規格 L 0.7mm

PCB Pad 設計 L 0.8mm

鋼網開孔建議 L0.5mm~0.6mm

適當內縮可以避免撐高造成高度影響

- Module Specifications L 0.7mm
- The design for PCB Pad : L:0.8mm
- We recommend the apertures for stencil L:0.5mm~0.6mm
- In order to avoid highness impact caused solder paste thickness, the stencil open size can be appropriately retracted

12. Package Information

12.1 Label

Label A → Anti-static and humidity notice



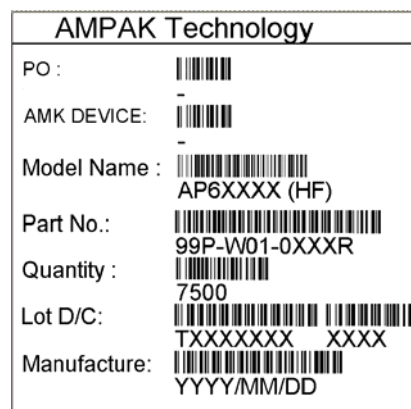
Label B → MSL caution / Storage Condition



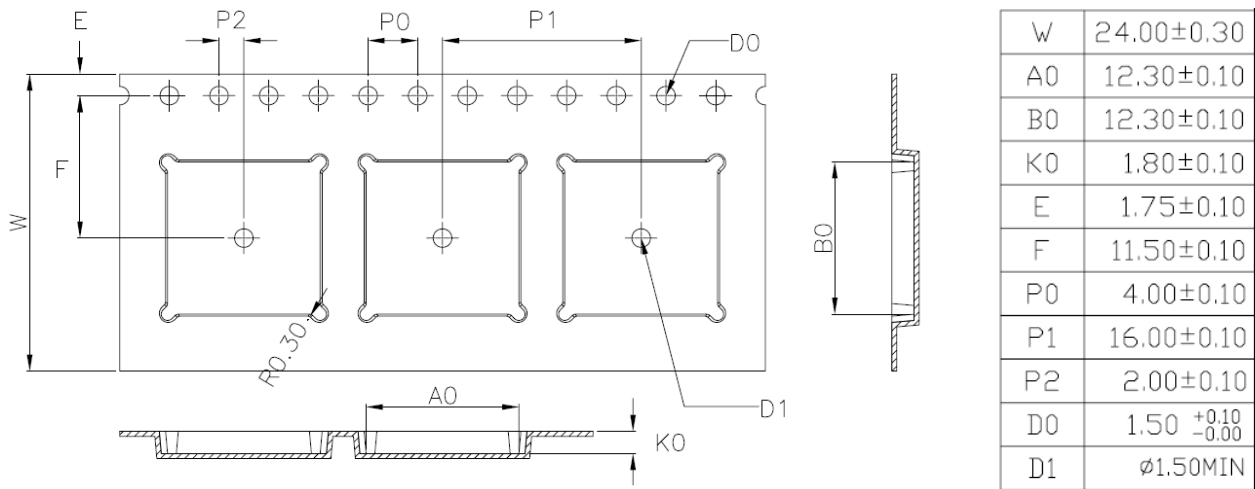
Label C → Inner box label .



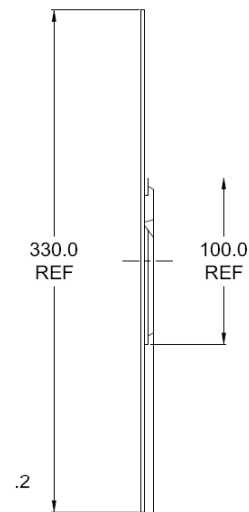
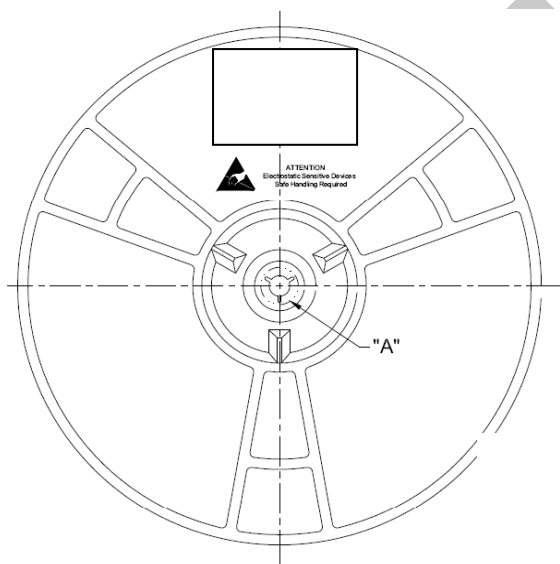
Label D → Carton box label .

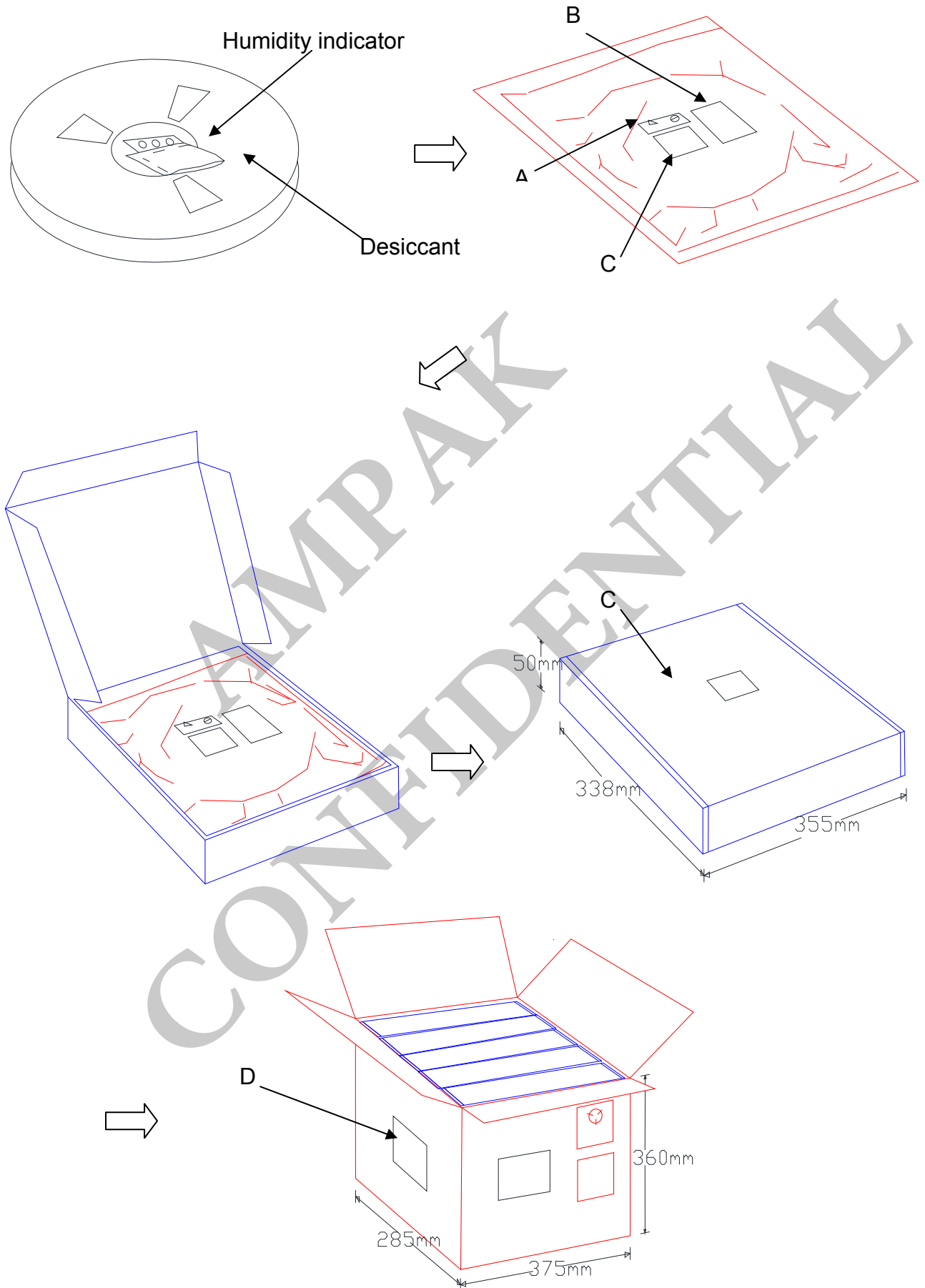


12.2 Dimension




1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





12.3 MSL Level / Storage Condition

	<p>Caution This bag contains MOISTURE-SENSITIVE DEVICES</p>	<p>LEVEL</p> <table border="1" style="margin: auto;"> <tr> <td style="text-align: center; padding: 10px;">4</td> </tr> </table> <p><small>If blank, see adjacent bar code label</small></p>	4
4			
<p>1. Calculated shelf life in sealed bag: 12 months at <math> < 40^{\circ}\text{C}</math> and <math> < 90\%</math> relative humidity (RH)</p>			
<p>2. Peak package body temperature: <u>250</u> $^{\circ}\text{C}$ <small>If blank, see adjacent bar code label</small></p>			
<p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be</p>			
<p>a) Mounted within: <u>72</u> hours of factory conditions <small>If blank, see adjacent bar code label</small></p> <p style="padding-left: 40px;">$\leq 30^{\circ}\text{C} / 60\% \text{ RH, or}$</p>			
<p>b) Stored per J-STD-033</p>			
<p>4. Devices require bake, before mounting, if:</p>			
<p>a) Humidity Indicator Card reads >10% for level 2a-5a devices or >60% for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$</p>			
<p>b) 3a or 3b are not met.</p>			
<p>5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.</p>			
<p>Bag Seal Date: _____ <small>If blank, see adjacent bar code label</small></p>			
<p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p>			

※NOTE : Accumulated baking time should not exceed 96hrs