11. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

External TCXO signal characteristics

Parameter	Specification	Units
Nominal input frequency	26	MHz
Signal type	Sine-wave	-
Input Voltage Swing	400-1900	mVp-p
Input Voltage	0-1800	mV
Input capacitance	6(max)	pF
Input Low	0-0.1VDD	V
Input High	0.9VDD-VDD	V
Duty cycle	40 - 60	%
Frequency Tolerance(initial accuracy)	±2	ppm
Frequency Stability	±0.5	ppm
Aging	±1	Ppm/year
Phase Noise(26Mhz@1KHz carrier offset)	-130(max)	dBc/Hz

11.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes It has the ability to stop the SDIO clock and map theinterrupt signal into a GPIO pin. This ‘out-of-band’ interrupt signal notifies the host when the WLANdevice wants to turn on the SDIO interface. The ability to force the control of the gated clocks fromwithin the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function1 Backplane Function to access the internal System On Chip (SOC) address space(Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)
- ❖

SDIO Pin Description

SDIO 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

12. Host Interface Timing Diagram

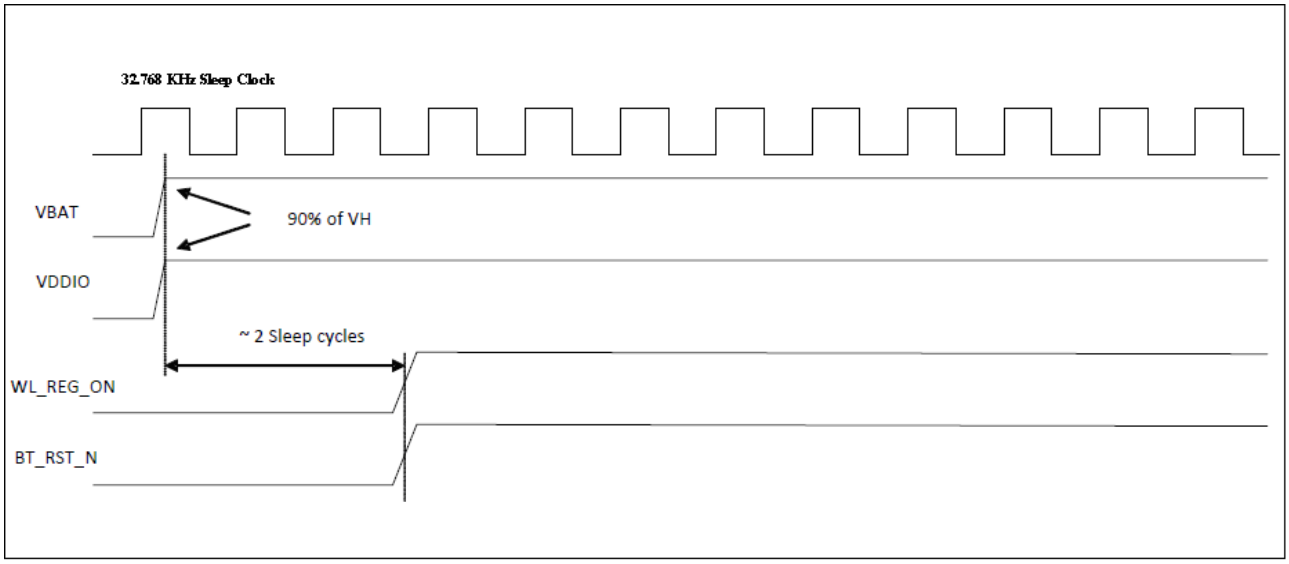
12.1 Power-up Sequence Timing Diagram

The module has two signals that allow the host to control power consumption by enabling ordisabling the Bluetooth/FM/GPS, WLAN and internal regulator blocks. These signals are described below.

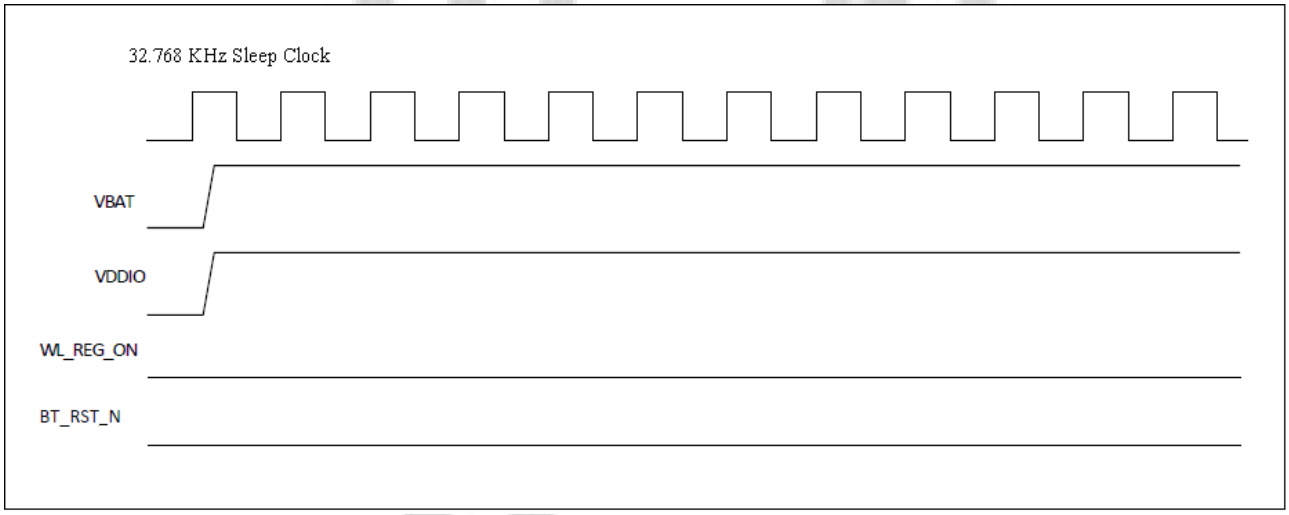
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operatingstates. The timing value indicated are minimum required values: longer delays are also acceptable.

Note that the WL_REG_ON and BT_RST_ON are in the module. The diagrams show bothsignals going high at the same time (as would be the case if both REG signals were controlled by asingle host GPIO). If two independent host GPIOs are used (on for WL_REG_ON and one forBT_REG_ON), then only one of the two signals needs to be high to enable the internal regulators.

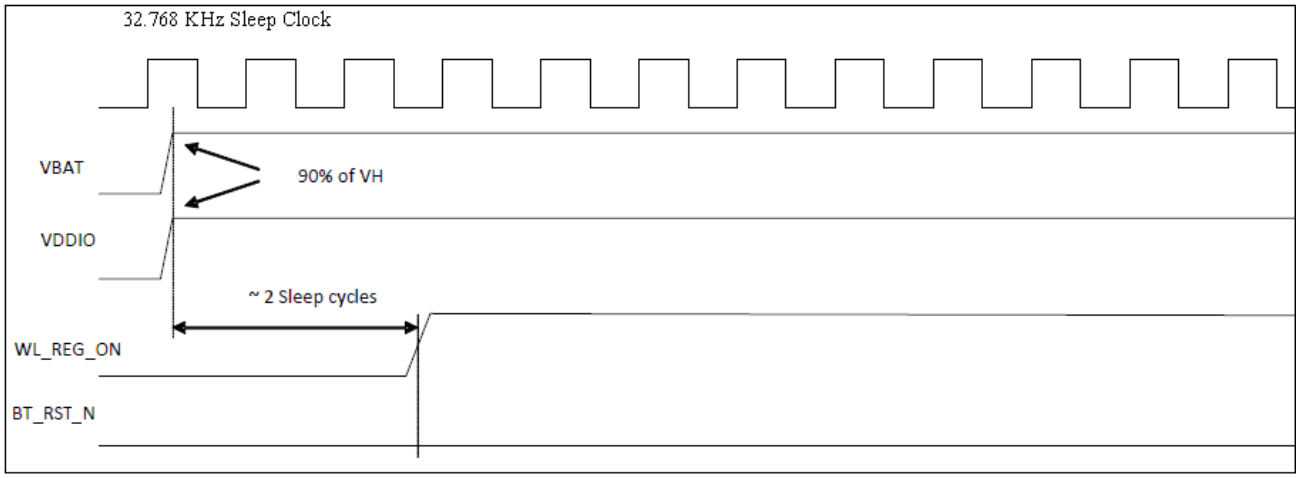
- ※ WL_REG_ON: Used by the PMU to power up the WLAN section. It is input to control the internal WLAN regulators. When this pin is high, the regulators are enabled andthe WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT_RST_ON:Used by the PMU to power up the internal Bluetooth/FM/GPS regulators. If the BT_RST_ON pins are low, the regulators are disabled.



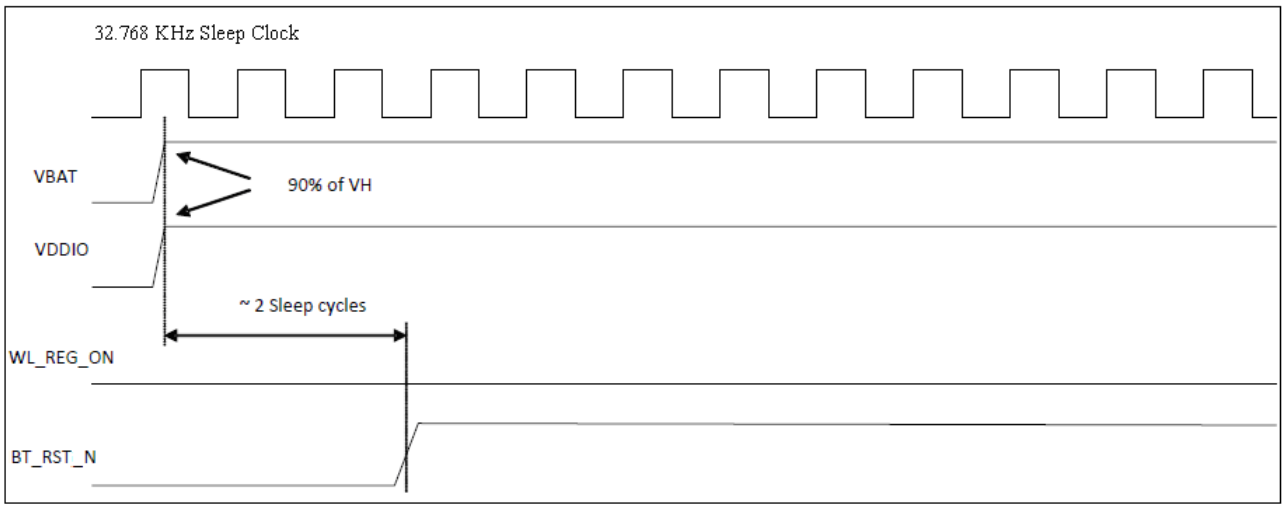
WLAN=ON, Bluetooth/FM/GPS =ON



WLAN=OFF, Bluetooth/FM/GPS =OFF

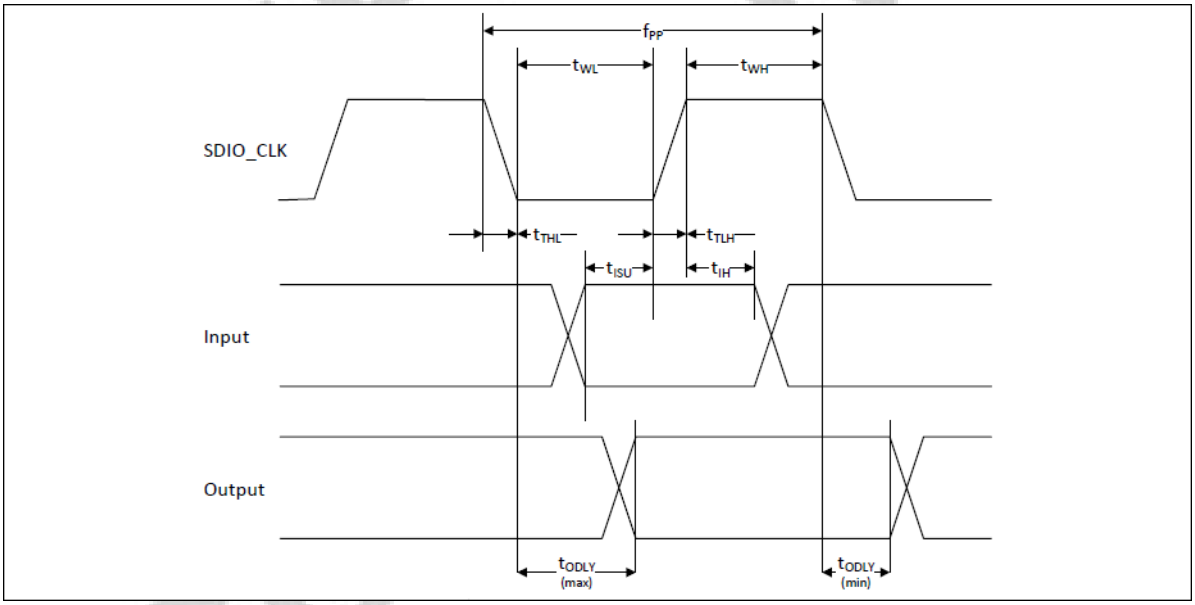


WLAN=ON, Bluetooth/FM/GPS=OFF



WLAN=OFF, Bluetooth/FM/GPS=ON

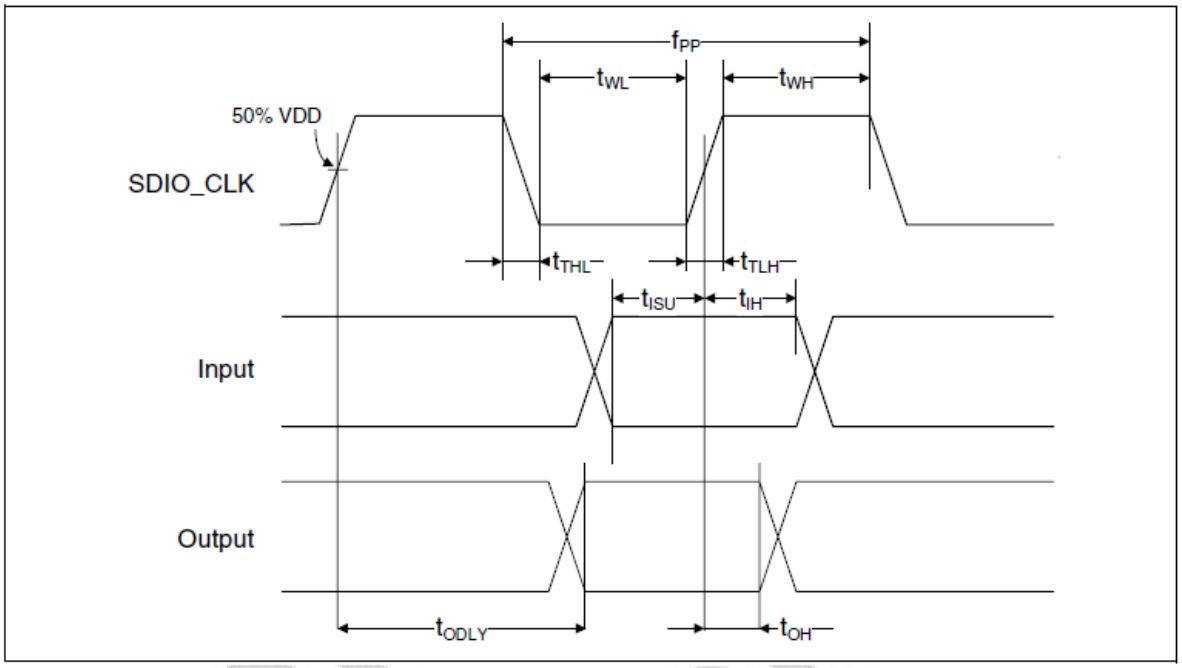
12.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

12.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

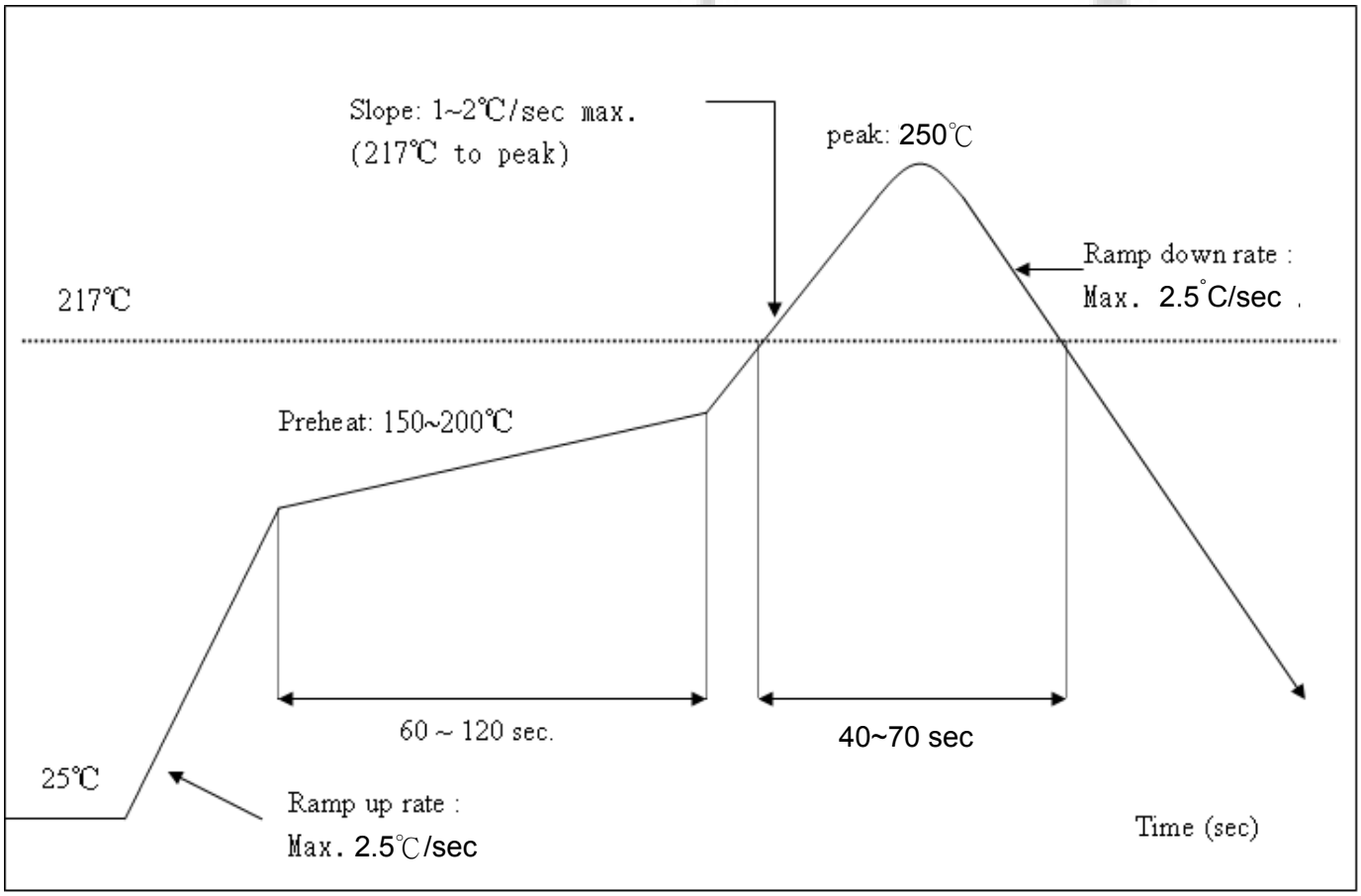
a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

13. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times

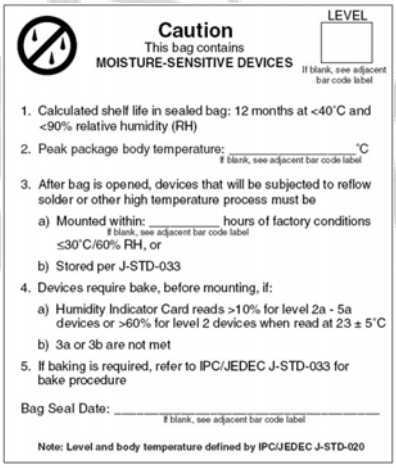


14. Package Information

14.1Label

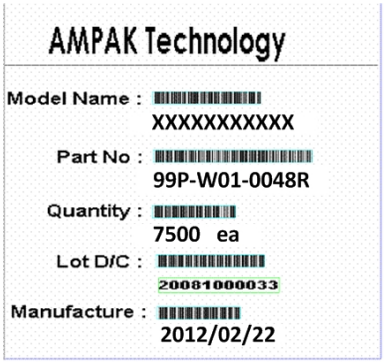
Label A→ Anti-static and humidity notice

Label B→ MSL caution / Storage Condition

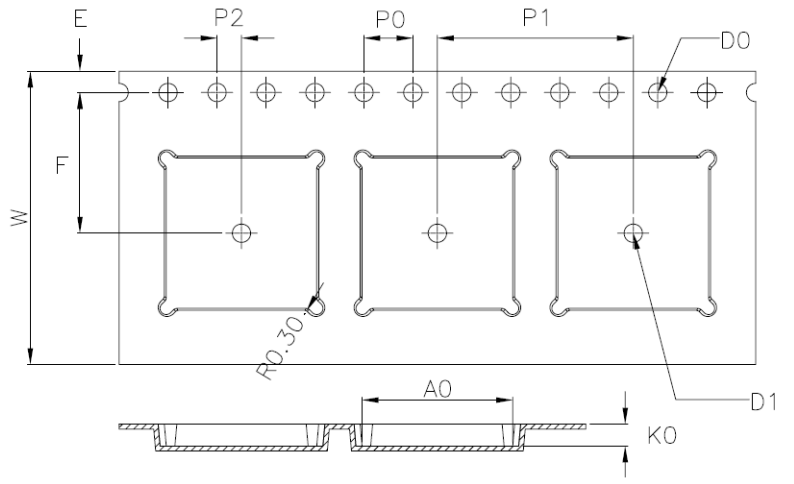


Label C→ Inner box label .

Label D→ Carton box label .

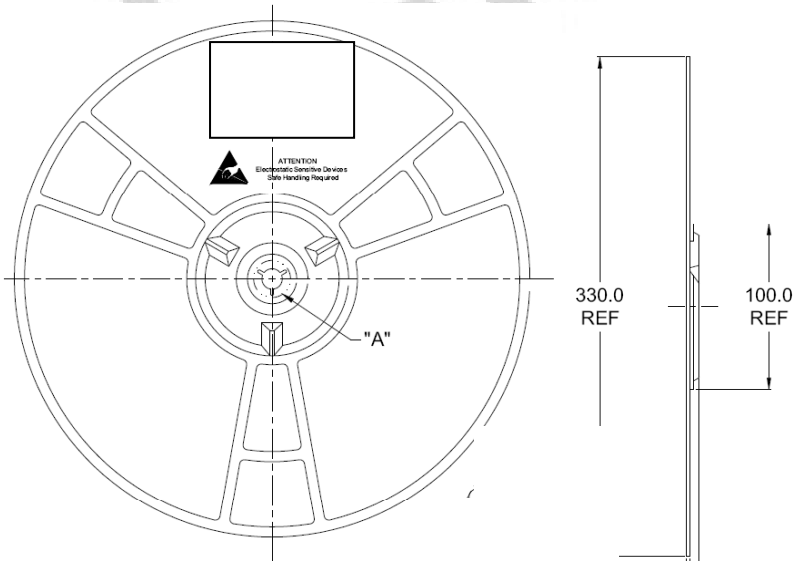


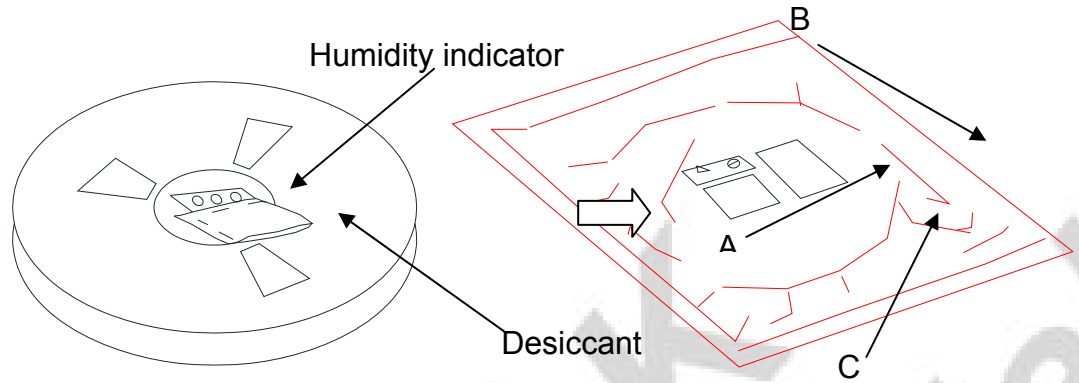
14.2Dimension

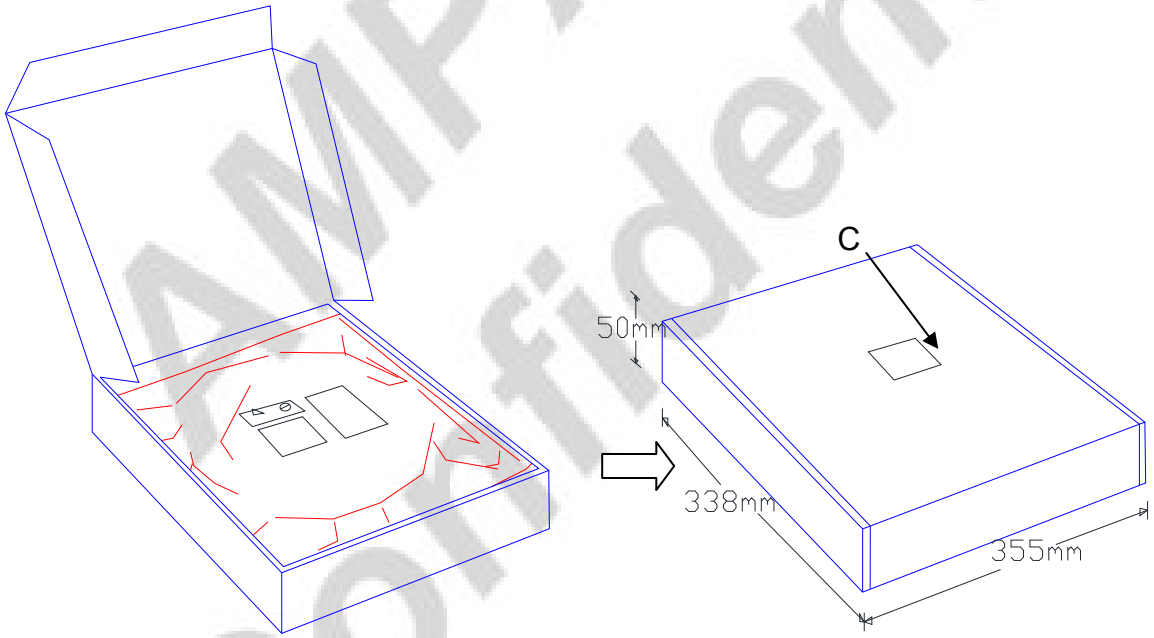


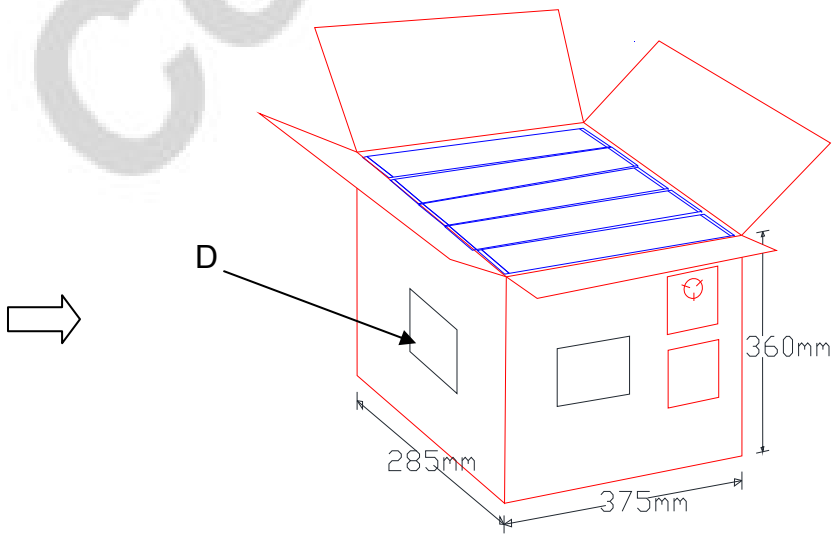
W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 $^{+0.10}_{-0.00}$
D1	ø1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.

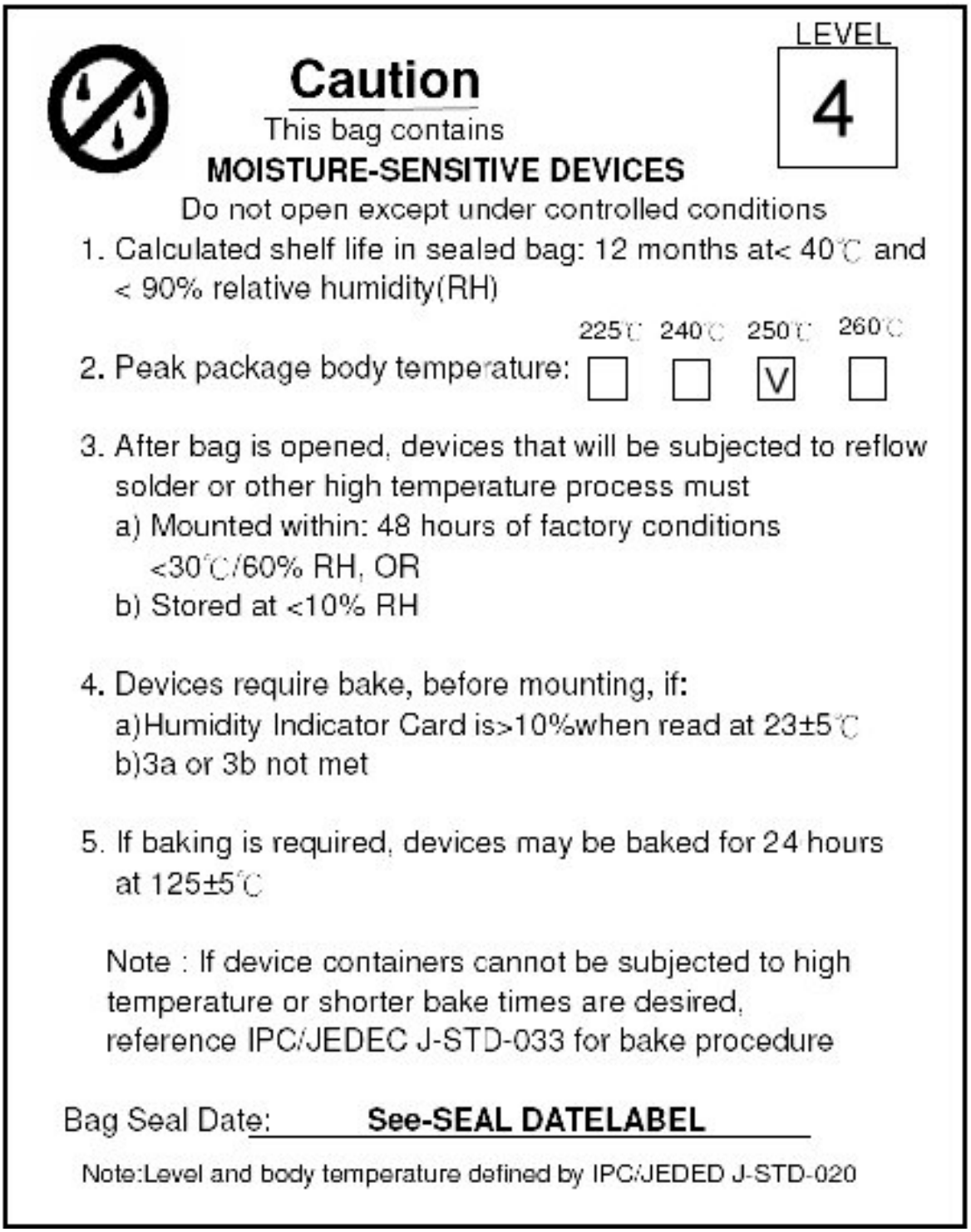








14.3 MSL Level / Storage Condition



※NOTE : Accumulated baking time should not exceed 96hrs